The paper HIGH-CAPACITY CAPACITORS FOR 0.5 VOLTAGE NANOELECTRONICS OF THE FUTURE was first published on Russian in journal «MODERN ELECTRONICS» («СОВРЕМЕННАЯ ЭЛЕКТРОНИКА») № 7, 2007, p. 24-29 (WWW.SOEL.RU)
Below, the text of paper on English is presented.

High-capacity capacitors for 0.5 voltage nanoelectronics of the future

Alexander Despotuli, Alexandra Andreeva (Moscow Region, Russia)

In nanoelectronics the demand on high-capacity capacitors of micron sizes sharply increases with a decrease of technological norms and power supply voltage (down to 0.5 V). Conventional capacitors do not possess required capacity density, radiation and temperature durability. The necessity of developing nanoionic supercapacitors (NSCs) based on advanced superionic conductors (AdSICs) and near future market demands on such devices are discussed.

Introduction

In portable devices, capacitors with their large size stand out sharply against other electronic components. With the development of nanoelectronics and critical technologies associated with it, creation of micro-scale capacitors and impulse storage devices with high density of energy (ρ_E), capacitance (ρ_C), and (ρ_W) power has become urgent.

The density of transitions in integrated circuits (IC) is limited by heat removal rather than by device sizes, therefore control over heat flows in present-day IC has stimulated the development of transistors with ultra-low supply voltage (V_{dd}). INTEL's processors have become of higher operation frequency and lower V_{dd} as the technology norms decreased (Fig.1).

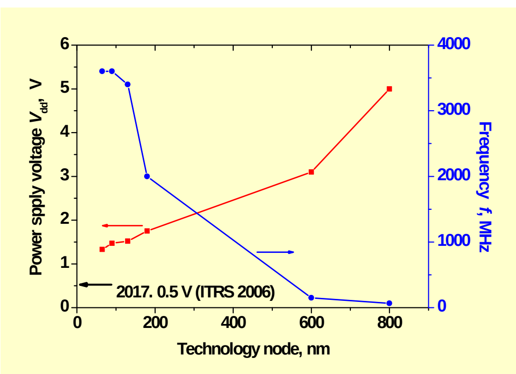

Fig.1. Frequency *f* and power supply voltage V_{dd} for INTEL's processors versus technological node [1].

Figure 2 presents a prognosis for changes in V_{dd} and gate length of CMOS transistors by 2020 (ITRS-2006). Basic technologies for nanoelectronics of near future have not been specified yet. One of possible technologies is InSb-based field effect transistors with V_{dd} =0.5 V [2].

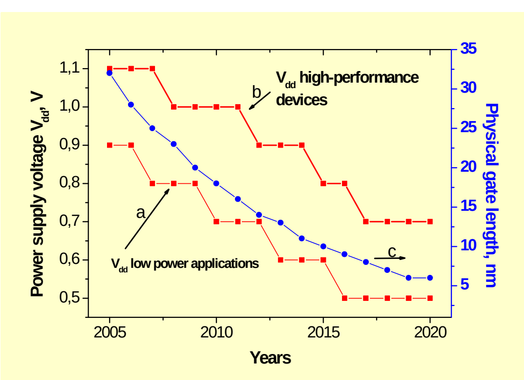

Fig.2. Prognosis for changes in V_{dd} and gate length for CMOS transistors (ITRS-2006).

- **a) low-power applications,**
- **b) high-performance devices,**
- **c) gate length.**

Reduction of energy consumption per 1 bit in microsystem and wireless technologies and small-scale digital devices of consumer electronics is a very urgent problem. Calculations show that for low power CMOS-devices, the minimum consumption is at $V_{dd} \leq 0.3$ V.

The basis for 0.5 voltage nanoelectronics can be

- low-voltage logic, memory and analog circuits [3,4];
- world's first 100 mV integrated CMOS [5];
- nanotube field-effect transistor with a high on/off ratio ($\sim 10^6$) and bias voltage ~0.5 V [6];
- field-effect for graphene (a novel promising 2D material whose properties combine chemical and mechanical stability) [7];
- molecular, one-dimensional nano-wire and hybrid devices;
- 0.4-volt nanoionic switches with quantum conductivity on the basis of superionic conductors [8].

The progress in integrated analog 0.4-0.5 V electronics has been described in the monograph [9].
Below, we present arguments for the use of solid state impulse supercapacitors with fast ion transport (FIT) in a double electric layer (DEL) on the functional advanced superionic conductor (AdSIC)/electronic conductor (EC) heterojunctions in the future 0.5 V nanoelectronics [10,11], wireless, microsystems and space technologies, RFID, high-temperature electronics and some other fields. These nanoionic supercapacitors (NSCs) can be fabricated by microelectronics technologies. Energy density and capacitance of NSC are 1-2 decimal orders of magnitude higher than in conventional-type capacitors with thin films of ferroelectric ceramics, SiO_2 , ZrO_2, HfO_2, etc. An inherent disadvantage of the conventional capacitors is exponential fast growth of tunnel leakage current at dielectric film thickness less than 2 nm. The frequency range of NSC operation is determined by FIT in DEL and has a theoretical limit of $\sim 10^{10}$ Hz (300 K), which corresponds to the frequency of jumps of mobile ions in AdSIC. High ρ_C in NSC (V_{dd} =0.5 V) is not associated with tunnel leakage current.

The order of NSC market cost magnitude can be evaluated by the formula:

$$V_{NSC} = \sum_j N^{(j)}_{IC} \cdot A^{(j)}_{IC} \cdot S, \qquad (1)$$

where V_{NSC} is the NSC gross cost, j is the market sector index, $N^{(j)}_{IC}$ is the number of IC produced, $A^{(j)}_{IC}$ is an average price of one IC, and S is an average fraction of the IC area taken by NSC. For example, in the RFID sector, the reservoir-capacitor of the power unit in modern IC takes approximately ¼ of the area, therefore $S \approx 0.25$ according to (1). The prognosis [12] for the period 2006-2016 says that the RFID market would increase by 10 times to cost $N^{(j)}_{IC} \cdot A^{(j)}_{IC} \sim \$ 26 \times 10^9$.

Fields of application of sub-voltage high-capacity micro-sized capacitors

In digital electronics, currents i on internal buses of IC increase as frequencies f increase and V_{dd} decrease. Large i gives rise to noise sources whose effect can be minimized by using decoupling capacitors C_{decap}. If the dissipated power is P = 100 W, f =1 GHz and V_{dd} =1.4 V, then

$$C_{decap} > 10\, P \cdot f^{-1} \cdot V^{-2}_{dd} . \qquad (2)$$

At low V_{dd} and high P, the value of $di/dt \approx P \cdot f \cdot V^{-1}_{dd}$ increases on the loaders. To prevent an increase in the voltage of a noise source, determined by di/dt , with respect to V_{dd} , the following steps should be taken

- to increase the area under C_{decap} (however , this reduces the efficiency and functioning of IC);
- to increase the density of capacitance δ_C (μF/cm^2) and ρ_C (μF/cm^3) of C_{decap} .

For nanodevices, 1/f noise (with spectral density $\sim \alpha N^{-1} f^{-1}$) is a fundamental challenge (N is the number of electron carriers in a sample). In perfect epitaxial layers, the constant α is $\sim 10^{-6}$ - 10^{-4}, in defect layers the constant is much higher. For example, in pMOSFET the 1/f noise increases by 10 to 100 times when the device size decreases from 350 to 130 nm [13]. A complex noise is filtered by several parallel-connected capacitors which differ in relaxation times τ , capacitance, inductance and equivalent resistance. Capacitors with large τ and ρ_C (δ_C) values are also used in low-frequency filters, amplifiers, seismic detectors, supply circuits, etc.

Tiny self-sustained objects of critical and advanced technologies require impulse energy and charge storage devices with high ρ_E, ρ_C and ρ_W values. Sub-voltage devices scavenged energy from the environment (light, pressure and temperature gradients, vibration, etc.) and β-radioisotope-based microgenerators together with impulse energy and charge storage devices can support long-term operation of portable devices of consumer electronics, wireless microsensors and microrobots networks, picosputnics, RFID, etc. According to *J.Pister*, the author of Smart Dust conception, autonomous power sources with $V_{dd} \leq 0.5$ V would be used in digital and analog electronics of self-sustained wireless networks with nodes which posses sensor, computation, and communication functions [14]. The incorporation of 3-V lithium cells into power units would require step-down DC/DC voltage converters which should contain high-capacity capacitors.

Present day 0.3 x0.3 x0.6 mm RFID chips include structures transforming radio-frequency energy into a direct current. In the simplest case, such structure is an antenna, a diode, and a reservoir-capacitor (δ_C ~0.35 μF/cm^2) determining the operation possibilities of a RFID chip.

The capacitance of a RFID chip reservoir-capacitor is determined by

$$C \approx i\ \Delta t\ (V_{max} - V_{min})^{-1} \ , \qquad (3)$$

where V_{max} and V_{min} are the limit voltage values, *I* is an average current on the load in the active stage of functioning, and Δt is the time of data transfer. In a future 0.5 V RFID, $\Delta V = V_{max} - V_{min}$ should be approximately 0.1 V, which radically differs from ΔV about 1 V in present-day chips.

The energy radiated by a RFID-chip $C\ V_{max}\ \Delta V$ and power $C\ V_{max}\ \Delta V\ /\Delta t$ depend on the distance and radio-exchange protocol. If V_{max} decreases by 3 times and ΔV by 10 times, the capacitance should increase by 30 times, so that $C\ V_{max}\ \Delta V$ product be retained, however a δ_C ~0.35 μF/cm^2 chip has no room to accommodate required capacitance. Most allowably would be *S* about 0.1, but conventional capacitors cannot afford δ_C ~50 μF/cm^2.

Operational frequencies of reservoir-capacitors are to correspond to the carrier frequency of radio exchange. In RFID standards, these are 135 kHz, 13.56 MHz, 2.45 GHz, 860-960 MHz, etc. So, 0.5 V RFID chips require capacitors with an operation frequency in the 10^5-10^9 Hz range. The condition δ_C ~50 μF/cm^2 determines the lower limit δ_C for many types of 0.5 V autonomous devices.

Modern design of micro-sized capacitors

Ferroelectric structures

For a plane capacitors, the voltage breakdown F_{max} , dielectric permittivity k , V_{dd} , ρ_C and δ_C are related as

$$V_{dd} = F_{max}\ (k\cdot \varepsilon_0\ /\rho_C\ )^{1/2} = F_{max}\ k\ \varepsilon_0/\delta_C\ , \qquad (4)$$

where ε_0 = 8.85 10^{-12} F m^{-1}. Therefore, devices with low V_{dd} stimulate the development of capacitors with limiting-high ρ_C (δ_C) determined by V_{dd} and tunnel leakage current (an "inherent" disadvantage of capacitors with dielectric layer thickness *d* less than 2 nm).

For sub-voltage electronics, promising are capacitors

- based on dielectrics with high *k* (ZrO_2 and HfO_2) characterized by $\delta_C \approx 2$ μF/cm^2 at $d \approx 2$ nm $V_{dd} \approx 1$ V [15];
- having trench structures (large aspect ratios), where the efficient $\delta_C \approx 3$ μF/cm^2 at the SiO_2 film thickness 4.5 nm [16] and $\delta_C > 20$ μF/cm^2 at the formation of dielectric layers with $k \approx 15...20$ [17];
- based on ferroelectric ceramics, e.g. PZT ($k \approx 900$), with $\delta_C \approx 3$ μF/cm^2 [18].

In nanoionic supercapacitors (NSC) based on AdSIC, F_{max} in a DEL (*d* of the atom size) can exceed 10^7 V/cm, therefore in smooth electrodes δ_C ~100 μF/cm^2 [11]. In NSC with trench structures, the effective values of δ_C ~1000 μF/cm^2.

The development of ferroelectric-based capacitors (*k* ~1000) have shown that *k* decreases considerably in thin films. Multilayer ferroelectric capacitors of ultra dense surface mount (UDSM) in a smallest case (01005 EIA) are of 0.4 x 0.2 x 0.2 mm size and maximum capacitance 0.01 μF at V_{dd} =6.3 V (ρ_C ≈1 μF/mm^3 and effective δ_C ≈13 μF/cm^2) [19]. Low-frequency capacitance of epitaxial heterostructures $ScRuO_3/ScTiO_3$ is approximately δ_C ≈26 μF/cm^2 which differs from the nominal value $\delta_C = \varepsilon_0 \cdot k / d$ =160 μF/cm^2 at k=490 and d =2.7 nm [20]. In capacitors based on perovskite thin films (5...30 nm), δ_C is usually equal to 12.5...2.5 μF/cm^2 (k ~70) at V_{dd} = 0.65...4.0 V [21].

Operation at temperatures higher than 85 ^{o}C is becoming conventional for small-size sources. A standard requirement to them is a guaranteed functioning of an electron component for 10 years at 125 ^{o}C. Multilayer ferroelectric capacitors operate at frequencies to 109 Hz and provide ρ_C ≈3 μF/mm^3 at the size 1.6 x 0.8 x 0.6 mm. Disadvantages of these capacitors are a reduction of ρ_C with increasing F and low stability of ceramics to higher temperatures and F [22]. So, present-day ferroelectric capacitors do not meet the requirements of δ_C - V_{dd} scaling and do not suit a number of critical technologies.

Miniature tantalum capacitors

High-capacity tantalum capacitors can operate at temperatures to 175 ^{o}C. The working voltage decreases with increasing temperature as follows: 6.3 v (85 ^{o}C), 4 V (125 ^{o}C), 3.2 V (150 ^{o}C), and 2.1 V (175 ^{o}C). Their capacity decreases in the range $10^3 \ldots 10^4$ Hz. When a 01005 case is used instead of a 3216 one, ρ_C decreases by 5…10 times (down to ρ_C ≈0.17…0.08 μF/mm^3). This effect is also characteristic of ferroelectric UDSM-capacitors.

Capacitors on the base of nanodielectrics with k ~10^7...10^{10}

A number of works [23,24] present experimental data on capacitors with nanodielectrics which are reportedly characterized by gigantic k ~10^7-10^{10} and a large potential in energy storage [24-26]. The analysis of data does not support the expectations.

In plane capacitor, the surface charge density δ_Q on atomically smooth electrodes is limited by $\delta_{C\ max}$ ~1.5 x 10^{-4} C/cm^2 (an ion charge of one sign on crystallographic planes with small indices, the concentration n ~ 10^{15} cm^{-3}), therefore

$$k \cdot F \leq \delta_{C\ max} / \varepsilon_0 \approx 1.5 \cdot 10^9 \text{ V/cm}, \qquad (5)$$

where $F = V/d$ and V is the voltage on electrodes.

According to (5), at k ~10^7 -10^{10} the maximum permissible value of $F_{\max}$ in a nanodielectric must be small (10^2 -10^{-1} V/cm) as compared to the breakdown field in ordinary dielectrics (≈2 x 10^6 V/cm). In the zero electrode thickness approximation, the maximum energy density in plane capacitors is

$$\rho_E \sim \varepsilon_0 \, k \, F^2_{\max} / 2 \quad . \qquad (6)$$

At $k \cdot F_{\max} \approx \delta_{Q\ max} / \varepsilon_0$, expression (6) can be written as

$$\rho_E < \sim \delta_{Q\ max} \, F_{\max}/2 \ , \qquad (7)$$

where $F_{\max}$ ~ 10^2 -10^{-1} V/cm. This shows that the expectations concerning the application of nanodielectrics with gigantic dielectric permittivity for energy storage are groundless.

Supercapacitors on the basis of liquid electrolytes

The possibility of using mobile ions for storing charge and energy has been realized in devices with a DEL, called supercapacitors. In the case of liquid electrolytes, electrodes with a large internal surface can provide ρ_C ~1000 μF/mm^3 (calculated per the internal surface area δ_C ~15 μF/cm^2 [27]), but the frequencies of device operation are low and the design of the devices is incompatible with vacuum technologies.

Advanced superionic conductors (AdSIC) – solid electrolyte (SE) and supercapacitors based on AdSIC-SE

Record high capacity-frequency characteristics can be obtained using coherent AdSIC/EC heterojunctions [28,29]. AdSIC have a crystal structure close to optimal for fast ion transport (FIT). The rigid ion sublattice of AdSIC has structure channels where mobile ions of opposite sign migrate. Figure 3 displays the distribution of Ag+-ion density in the conduction channels of $RbAg_4I_5$ AdSIC (300 K) [30]. The ion-transport characteristics of AdSIC are very high, ionic conductivity σ_i ≈0.3 Ohm^{-1} cm^{-1} ($RbAg_4I_5$, 300 K) and activation energy E_i ≈0.1 eV. This determines the temperature-dependent concentration of mobile ions

$n_i \sim N_i \exp (E_i / k_B T)$ capable to migrate in conduction channels at each moment ($N_i \approx 10^{22}$ cm^{-3}, $n_i \sim 2 \cdot 10^{20}$ cm^{-3}, 300 K).

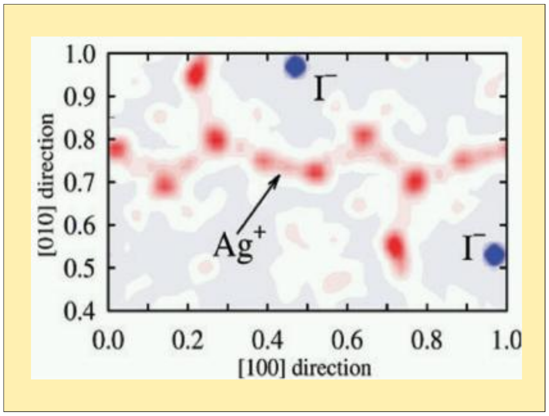

Fig.3. Time-averaged distribution of Ag^+ density in the channels of ionic conductivity of AdSIC (crystal structure of $RbAg_4I_5$) [30].

The general classification of solid state ionic conductors according to their ion-electron conductivities (σ_i - σ_e) is presented in Fig. 4 [10,28]. The boundary of the 7-8 area determines the upper limit of σ_I values for hypothetic AdSIC. By definition, these ionic conductors should have $E_i \approx k_B T$ (300 K), which is to give at 300 K $\sigma_i \sim 2$ Ohm^{-1}cm^{-1} (mobile Ag^+-ions) and $\sigma_i \sim 8$ (20) Ohm^{-1}cm^{-1} for mobile Li^+ (H^+) ions.

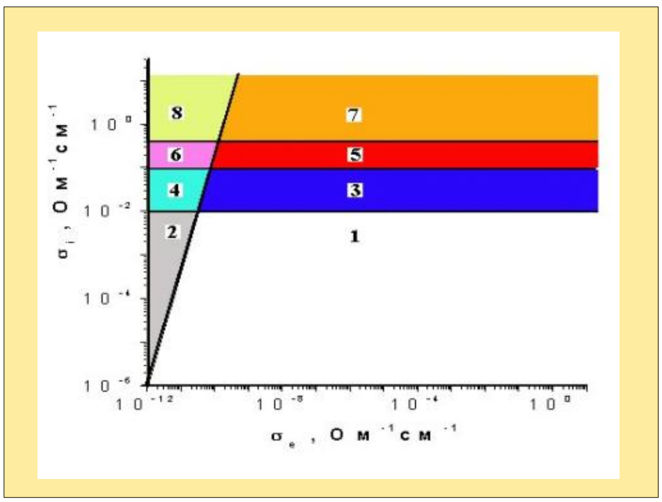

Fig.4. Classification of solid state ionic conductors in the lgσ_i - lgσ_e coordinates (Ohm^{-1} cm^{-1}) [10].
2, 4 and 6 – known solid electrolytes (SEs), materials with $\sigma_i >> \sigma_e$;
1, 3, and 5 – known mixed ion-electron conductors;
3 and 4 – superionic conductors (SICs), i.e. materials with $\sigma_i > 0.001$ Ohm^{-1}cm^{-1}, σ_e – arbitrary value;
4 – SIC and simultaneously SE, $\sigma_i > 0.001$ Ohm^{-1}cm^{-1}, $\sigma_i >> \sigma_e$;
5 and 6 – advanced superionic conductors (AdSICs), where $\sigma_i > 10^{-1}$ Ohm^{-1}cm^{-1} (300 K), $E_i \approx 0{,}1$ eV, σ_e – arbitrary value;
6 – AdSIC and simultaneously SE, $\sigma_i > 10^{-1}$ Ohm^{-1}cm^{-1}, $E_i \approx 0{,}1$ eV, $\sigma_i >> \sigma_e$;
7 and 8 – hypothetical AdSIC with $E_i \approx k_B T \approx 0.03$ eV (300 K);
8 – hypothetical AdSIC and simultaneously SE.

The $RbAg_4I_5$ family includes a number of ADSIC-SE with Cu^+ or Ag^+ mobile ions. Some of these compounds are thermodynamically stable around room temperature (α-$RbAg_4I_5$, $CsAg_4I_{2-x}I_{3+x}$, $RbCu_4Cl_3I_2$, etc.) but the majority of them are stable at higher temperatures (50-120 °C).

ADSIC-SE –based supercapacitors have already been developed for several decades (their radiation stability can be 4 Y), however, the δ_C of their heterojunctions (with arbitrary, structure-uncontrolled AdSIC/EC heteroboundaries) is 10^2 -10^1 μF/cm^2 at frequencies 10^{-2} -10^3 Hz. Low operation frequencies of AdSIC/EC heterojunctions and, hence, low ρ_W of supercapacitors are the result of FIT violation in molecular-thin DEL on the ADSIC/SE heteroboundaries. The product of maximum operation frequency f_{Max} of ADSIC/EC heterojunction by δ_C is a generalized characteristic of capacity and frequency parameters. For typical heterojunctions, e.g. $RbAg_4I_5$/Pt [31], this product $f_{Max} \cdot \delta_C$ is ~ 1 -10^4 Hz μF/cm^2. For heterojunctions with liquid electrolytes, the $f_{Max} \cdot \delta_C$ product is of the same order of magnitude.

Research and development in nanoionics of AdSIC, a new science and technological field, have been carried on at the Institute of Microelectronics Technology RAS for some years [28]. The object of these investigations is nano- and microstructures based on AdSIC. AdSIC/EC heterojunctions are key functional structures in devices with a DEL. The effect of heteroboundaries on ion transport in these devices is of determining character, therefore the major approach to ADSIC nanoionics is to retain the concentration and potential barrier heights to mobile ion jumps on heteroboundaries at the level of those in ASIC volume.

Creation of model film impulse device on the basis of AdSIC

High values of $f_{Max} \cdot \delta_C$ on AdSIC/EC heterojunctions can be obtained under certain conditions. These are

- to form an atomically clear and sharp AdSIC/EC contact;
- to provide small disordering of the structure in an AdSIC layer adjacent to EC, which can be realized on the AdSIC/EC coherent boundaries;
- to provide a certain combination and mutual arrangement of crystal symmetry elements of the AdSIC/EC heteroboundary and symmetry elements of FIT channels in the AdSIC structure.

To his end, methods of crystallochemical design of AdSIC/EC heteroboundaries were employed [28,29]. AdSIC/EC heterostructures (prototypes of NSC) were developed and synthesized with $\delta_C \approx 100$ μF/cm^2 and $f_{Max} \sim 10^6$ Hz (record high values of the product $f_{Max} \cdot \delta_C \sim 10^8$ Hz μF/cm^2) [10,11].

Figure 5 shows frequency-capacity characteristics $\delta_C = \delta_C(f)$ for a typical AdSIC/EC heterojunction ($RbAg_4I_5$/Pt [31]) created without taking into account the three above conditions and for an experimental two-electrode cell based on AdSIC [10,11].

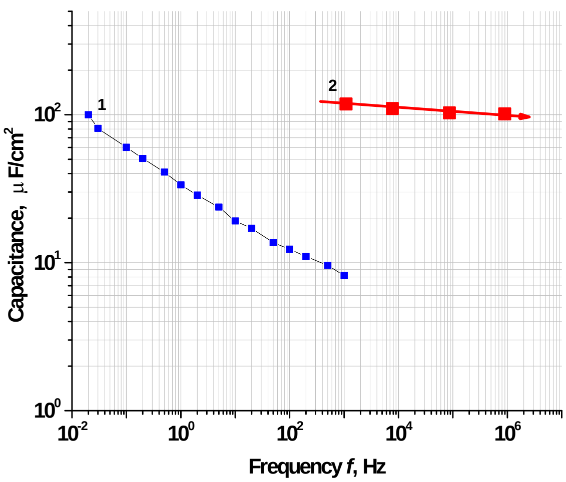

Fig. 5. Frequency-capacitance characteristic. A typical AdSIC/EC heterojunction ($RbAg_4I_5$/Pt, 20 °C, plot 1) and the experimental two-terminal cell on the basis of AdSIC (155 °C, plot 2).

The frequency-capacity characteristics [10,11] were obtained by comparing "charge-discharge" oscillograms for the experimental two-electrode cell and a standard capacitor. The Π-impulses of an external voltage were applied to a circuit consisting of the experimental cell (or a standard capacitor) and a ballast resistor *R* connected in series. The experimental cell of ≈0.0036 mm^3 volume (01005 UDSM component has the volume ≈0.016 mm^3) had thin film electrodes of the total area ≈0.08 mm^2 (0.04 mm^2 + 0.04 mm^2). The cell thickness was ≈0.03 mm, the area of the cell footprint on the Si-substrate ~0.12 mm^2.

Voltage changes during "charge-discharge" processes in the experimental cell and the standard capacitor are shown in Figs. 6. Changes in the charge (discharge) time were set by the ballast resistor *R*.

The effective δ_C in the experimental cell is ≈1 μF/mm^2 (100 μF/cm^2) at frequencies to ≈10^6 Hz (Fig.6) and the power density $\rho_W \approx 0.3$ W/mm^3 (3·10^2 W/cm^{-3}). This is 3 times greater than in massive supercapacitors which have distributed carbon electrodes impregnated by a liquid electrolyte (volume ~1 cm^3, $V_{dd} \approx 2.5$ -2.7 V, operation frequencies not higher than $f_{Max} < 10^3$ Hz). The energy density ρ_E in the cell is ≈10^{-4} J/mm^3 (10^{-1} J/cm^{-3}). This is of 36 times smaller than in massive supercapacitors where the product $\rho_W \cdot \rho_E \sim 4 \cdot 10^2$ J^2 /s cm^6 (in the cell, this product is 10 times smaller). However, by changing the cell design, the volume can be reduced by 10 times while retaining the stored energy and generated power at the same level. As a result, the product $\rho_W \cdot \rho_E$ could exceed that of massive supercapacitors by ≈10 times at the ≈0.0004 mm^3 volume.

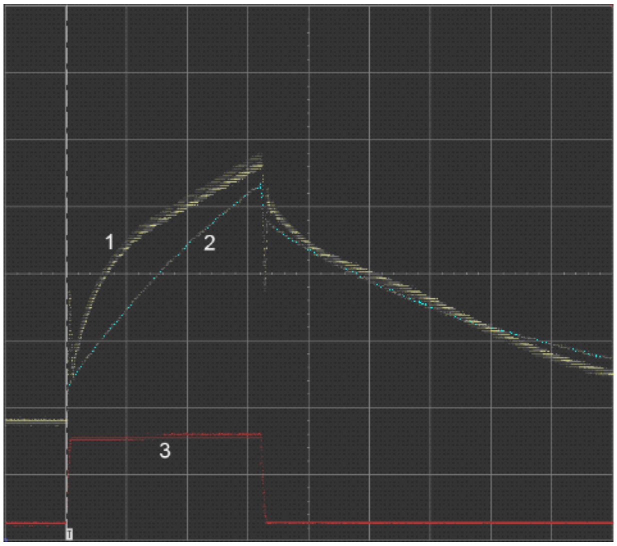

Fig. 6. Time dependence of the voltage (horizontal scale 1 μs/div) during the charge-discharge process in the two-terminal experimental cell and the 0.047 μF capacitor through the ballast resistor R=100 Ohm: 1) the cell at 155 ^{o}C; 2) 0.047 μF capacitor connected in series to the resistor *r* =10 Ohm (vertical scale 100 mV/Div; 3) voltage from an external generator (vertical scale 500 mV/div) for the cases (1) and (2).

Experiments with the ≈0.0036 mm^3 cell showed that

- effective capacitance density δ_C depends rather weakly on *f* up to frequencies ≈10^6 Hz (Fig.5)
- δ_C increases with voltage at the cell voltage *U* > 0.2 V
- the cell can operate for a long time at 70–170 ^{o}C
- δ_C ≈1 μF/mm^2, ρ_C >10 μF/mm^3, ρ_W ≈0.3 W/mm^3, and $\rho_E \approx 10^{-4}$ J/mm^3 can be obtained at frequencies ≈10^6 Hz.

So, film impulse capacitors based on AdSIC are promising devices for 0.5 V electronics and some critical technologies.

Conclusion

In nanoelectronics, the reduction in technological norms and supply voltage (down to 0.5 V by 2016-2020, ITRS-2006) drastically increases the demand on high-capacity capacitors of micron-sizes (filtration of interferences and low-frequency 1/*f* noise, smoothing of impulses, supplying of impulse loads at low (~0.1V) permissible voltage drops, operation at elevated temperatures and under penetrating ionization radiation, etc.). Giant investments into *R&D* of tradition design capacitors have not resulted in a considerable increase of capacity density, radiation and temperature durability of such devices.

An alternative concept is proposed of wide usage of impulse AdSIC-based nanoionic supercapacitors in the sub-voltage electronics and critical technologies associated with it (wireless sensor and microrobot networks, microsystem and space technologies, high-temperature electronics, RFID, etc.). In the authors' opinion, the development of NSC would start a new field of novel knowledge and technologies and bring about radical changes in the market of advanced nanoelectronics and high-tech consumer goods of mass production.

Addition for English version of paper

NSCs are in demand for sub-voltage nanoelectronics-2017 and beyond. An inevitable appearance of new ICs operating near the theoretical limit on energy consumption per 1 bit processing, i.e. at V_{dd} < 0.2 V, would also require an increase in capacity density.

Following G. Moore, the challenge can be designated by the words: "*Cramming more capacitance onto integrated circuits!*" The authors call attention to the possibility of large-scale enterprise on the NSC *R&D* and commercial activities.

References

1. *Grochowski E., Annavaram M.* Energy per instruction trends in Intel microprocessors // Technology@Intel Magazine. March 2006. P. 1-8.
2. *Chau R., Datta S., Majumdar A.* Opportunities and challenges of III-V nanoelectronics for future high-speed, low-power logic application // Compound Semiconductor Integrated Circuit Symposium 2005.
3. *Ishibashi K., Fujimoto T., Yamashita T., Okada H., Rima Y., Hashimoto Y., Sakata K., Minematsu I., Itoh Y., Toda H., Ichihashi M., Komatsu Y., Hagiwara M., Tsukada T.* Low-voltage and low-power logic, memory, and analog circuit techniques for SoCs using 90 nm technology and beyond // IEICE Trans. Electron. 2006. V..E89–C. #.3. P.250-262.
4. *Morita Y., Fujiwara H., Noguchi H., Kawakami K., Miyakoshi J., Mikami S., Nii K., Kawaguchi H., Yoshimoto M.* A 0.3-V operating, V_{th}-variation-tolerant SRAM under DVS environment for memory-rich SoC in 90-nm technology era and beyond // IEICE Trans. Fundamentals 2006. V. E89–A, P. 3634-3641.
5. www.hitachi.com/New/cnews/E/2002/0205/0205.pdf
6. *Javey A., Tu R., Farmer D.B., Guo J., Gordon R.G., Dai H.* High performance n-type carbon nanotube field-effect transistors with chemically doped contacts // Nano Letters 2005. V.5. P. 345-348.
7. *Lemme M.C., Echtermeyer T.J., Baus M., Kurz H.* A graphene field-effect device // IEEE Electron Device Letters 2007. V.28. P.282-284.
8. *Banno N., Sakamoto T., Iguchi N., Kawaura H., Kaeriyama S., Mizuno M., Terabe K., Hasegawa T., Aono M.* Solid-electrolyte nanometer switch // IEICE Trans. Electron. 2006. V.E89–C. P. 1492-1498.
9. *Chatterjee S., Pun K.P., Stanic N., Tsividis Y., Kinget P.* Analog Circuit Design Techniques at 0.5V // Springer. 2007. 158 P.
10. *Despotuli A., Andreeva A.* Supercapacitors for electronics // Modern Electronics (Rus) 2006. №5. P.10 -16.
11. *Despotuli A.L., Andreeva A.V., Vedeneev V.V., Aristov V.V., Malsev P.P.* High-capacity capacitors for ultra-dense surface mount // Journal of Nano- and Microsystems Techniques (Rus) 2006. № 3. P. 30-37.
12. www.idtechex.com
13. *Chew W., Yeo K. S.,Chu S. -F.* Effect of technology scaling on the 1/f noise of deep submicron PMOS transistors // Solid-State Electronics 2004. V. 48. P. 1101-1109.
14. www.dustnetworks.com
15. *Gusev E. P., Narayanan V., Frank M. M.* Advanced high-k dielectric stacks with poly Si and metal gates: Recent progress and current challenges // IBM J. Res. Dev. 2006. V. 50. NO. 4/5. P. 387-410.
16. *Black C.T., Guarini K.W., Zhang Y., Kim H., Benedict J., Sikorski E., Babich I.V., Milkove K.R.* High-capacity, self-assembled metal–oxide–semiconductor decoupling capacitors // IEEE Electron Device Lett. 2004. V. 25. NO.9. P. 622-624.
17. *Klootwijk J., Kemmeren A., Wolters R., Roozeboom F., Verhoeven J., Heuvel E.* Extremely high-density capacitors with ALD high-*k* dielectric layers // NATO Science Series II: Mathematics, Physics and Chemistry. V. 220. 2006. P. 17-28.
18. www.st.com/stonline/press/news/year2005/t1701d.htm
19. *Hisaki T.* Murata's technology paves way for ultra-small capacitors // AEI May 2004. P. 43-44.
20. *Stengel M., Spaldin N.A.* Origin of the dielectric dead layer in nanoscale capacitors // Nature 2006. V. 443. P. 679-682.
21. *Jo J.Y., Kim Y.S., Kim D.H., Kim J.D., Chang Y.J., Kong J.H., Park Y.D., Song T.K., Yoon J.-G., Jung J.S., Noh T.W.* Thickness-dependent ferroelectric properties in fully-strained $SrRuO_3/BaTiO_3/SrRuO_3$ ultra-thin capacitors // Thin Solid Films 2005. V. 486. P. 149-152.
22. *Tsubota S.* High-capacitance capacitors by Murata make smaller power supplies // AEI December. 2005. P. 41-43.
23. *Saha S.K., Chakravorty D.* One-dimensional organic giant dielectrics // Appl. Phys. Lett. 2006. V. 89. P. 043117-1 - 043117-3.
24. *Saha S.K., DaSilva M., Hang Q., Sands T., Janes D.B.* A nanocapacitor with giant dielectric permittivity // Nanotechnology 2006. V.17. P. 2284-2288.
25. *Cao Y., Irwin P.C., Younsi K.* The future of nanodielectrics in the electrical power industry // IEEE Trans. on Dielectrics and Electrical Insulation 2004. V.11. P. 797-807.
26. Air force STTR 06 T002 topic descriptions. Nanodielectrics for high power capacitors and passive applications // www.acq.osd.mil/osbp/sbir/solicitations/sttr06/af06.htm
27. *Chmiola J., Yushin G., Gogotsi Y., Portet C., Simon P., Taberna P. L.* Anomalous increase in carbon capacitance at pore sizes less than 1 nanometer // Science 2006. V. 313. P. 1760-1763.
28. *Despotuli A.L., Andreeva A.V., Rambabu B.* Nanoionics of advanced superionic conductors // Ionics 2005. V. 11. P. 1-9.
29. *Andreeva A.V., Despotuli A.L.* Interface design in nanosystems of advanced superionic conductors // Ionics.2005. V.11.№.1&2.P. 152-160.
30. *Hull S.* Superionics: crystal structures and conduction process // Rep. Prog. Phys. 2004. V.67. P.1233-1314.
31. *Karamov F.A.* Superionic conductors. Heterostructures and elements of functional electronics //M. «Science press» (Rus) 2002. 237 P.

The Laboratory of Nanoionics,
Institute of Microelectronics Technology and High Purity Materials, Russian Academy of Sciences (IMT RAS)
142432 Chernogolovka, Moscow Region, Russia
despot@ipmt.ru